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Semiconductor Electronics — CBSE Class 12 Physics Chapter Test

FREE CHAPTER TEST · CLASS XII · PHYSICS (042) · PATTERN OF THE CBSE SAMPLE QUESTION PAPER 2026-27

TIME ALLOWED	MAXIMUM MARKS	QUESTIONS	NAME / ROLL NO.
1½ hours	37	17 (A 8 · B 3 · C 3 · D 1 · E 2)	

GENERAL INSTRUCTIONS

Read the following instructions very carefully and strictly follow them:

1. This question paper contains 17 questions. All questions are compulsory.
2. This question paper is divided into five sections: A, B, C, D and E.
3. Section A (Q1–8) contains 6 multiple choice questions and 2 assertion-reason based questions of 1 mark each.
4. Section B (Q9–11) contains short answer questions of 2 marks each.
5. Section C (Q12–14) contains short answer questions of 3 marks each.
6. Section D (Q15) contains case study based questions of 4 marks each, with four sub-parts of 1 mark.
7. Section E (Q16–17) contains long answer questions of 5 marks each.
8. There is no overall choice. However, an internal choice has been provided in 1 question in Section B, 1 question in Section C, 2 questions in Section E. Attempt only one of the alternatives in such questions.
9. Use of calculators is not allowed. You may use: $e = 1.6 \times 10^{-19}$ C.
10. This chapter test follows the section structure, question types and marks per question of the CBSE Class XII Physics (042) Sample Question Paper 2026-27, at about half the length of the 70-mark board paper: 37 marks in 1½ hours.
11. The answer key and the marking scheme are at the end of this booklet. Attempt the paper in 1½ hours before you look at them.

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Chapter: Semiconductor Electronics · **Topics:** Energy bands · Intrinsic and extrinsic semiconductors · p-n junction and depletion layer · Diode characteristics · Diode as a rectifier

SECTION A

This section comprises 8 questions of 1 mark each: 6 multiple choice questions (MCQs) and 2 assertion-reason based questions.

1. To make an n-type semiconductor, pure silicon should be doped with 1

(A) boron (B) aluminium

(C) indium (D) phosphorus

2. In an intrinsic semiconductor at room temperature, the concentrations of free electrons n_e and holes n_h are related by 1

(A) $n_e = n_h$ (B) $n_e > n_h$

(C) $n_e < n_h$ (D) $n_e = n_h = 0$

3. The energy band gap of silicon is about 1

(A) 0.01 eV (B) 6 eV

(C) 1.1 eV (D) 13.6 eV

4. The majority charge carriers in a p-type semiconductor are 1

(A) free electrons (B) holes

(C) positive ions (D) negative ions

5. When a p-n junction is forward biased, its depletion layer 1

(A) becomes narrower (B) becomes wider

(C) does not change (D) becomes wider and the barrier rises

6. A full-wave rectifier is supplied with 50 Hz AC. The fundamental frequency of the ripple in its output is 1

(A) 25 Hz (B) 50 Hz

(C) 100 Hz (D) 200 Hz

7. **Assertion (A) :** The resistance of a semiconductor decreases as its temperature rises. 1
Reason (R) : Doping silicon with a trivalent impurity makes it a p-type semiconductor.

(A) Both Assertion (A) and Reason (R) are true and Reason (R) is the correct explanation of Assertion (A).

(B) Both Assertion (A) and Reason (R) are true, but Reason (R) is not the correct explanation of Assertion (A).

(C) Assertion (A) is true, but Reason (R) is false.

(D) Assertion (A) is false and Reason (R) is also false.

8. **Assertion (A) :** A p-type semiconductor carries a net positive charge. 1

Reason (R) : In a p-type semiconductor, the number of holes equals the number of free electrons.

(A) Both Assertion (A) and Reason (R) are true and Reason (R) is the correct explanation of Assertion (A).

(B) Both Assertion (A) and Reason (R) are true, but Reason (R) is not the correct explanation of Assertion (A).

(C) Assertion (A) is true, but Reason (R) is false.

(D) Assertion (A) is false and Reason (R) is also false.

SECTION B

This section comprises 3 short answer questions of 2 marks each.

9. Pure silicon has an intrinsic carrier concentration of 1.0×10^{16} m^{-3} and 5.0×10^{28} atoms per m^3. It is doped with boron at 1 atom per 10^7 silicon atoms. Find the hole and electron concentrations. Is it n-type or p-type? 2

10. (a) Explain how the depletion region and the barrier potential are formed at a p-n junction. 2

OR

(b) Why does a pure semiconductor behave as an insulator at 0 K but conduct a little at room temperature?

11. A silicon diode (forward voltage drop 0.70 V) is connected in series with a 200 Ω resistor to a 5.0 V battery so that the diode is forward biased. Find the current. What is the current if the battery is reversed? 2

SECTION C

This section comprises 3 short answer questions of 3 marks each.

12. (a) With the help of a circuit diagram (described in words), explain the working of a half-wave rectifier. Describe the input and output waveforms. 3

OR

(b) (i) Describe the V-I characteristics of a silicon p-n junction diode in forward and reverse bias.
(ii) The forward current of a diode is 10 mA at 0.70 V and 20 mA at 0.75 V. Find its dynamic resistance in this range.

13. Two ideal diodes D_1 and D_2 are in separate branches, each in series with a 100 Ω resistor, and both branches are connected in parallel across a 10 V battery. D_1 is forward biased and D_2 is reverse biased. Find (i) the current in each branch and (ii) the current drawn from the battery. (iii) What are the currents if the battery is reversed? 3

14. (i) What happens to the width of the depletion layer and to the barrier at a p-n junction when it is reverse biased? 3
(ii) Why is the reverse current very small and nearly independent of the reverse voltage?
(iii) What happens if the reverse voltage is made very large?

SECTION D

This section comprises 1 case study based question of 4 marks, with four sub-parts of 1 mark each.

15. A phone charger turns 230 V, 50 Hz mains into a low DC voltage. A small transformer first lowers the voltage; then four diodes connected in a bridge change the AC into pulsating DC; finally a capacitor connected across the output smooths it before it reaches the phone.

(I) The four-diode bridge performs
(A) amplification (B) half-wave rectification (C) full-wave rectification (D) voltage step-up [1]

(II) The fundamental frequency of the pulsating DC from the bridge is
(A) 100 Hz (B) 50 Hz (C) 25 Hz (D) 0 Hz [1]

(III) The capacitor across the output is used to
(A) increase the frequency (B) store charge permanently (C) change DC back to AC (D) reduce the ripple and smooth the output [1]

(IV) In each half cycle, the number of diodes of the bridge that conduct is
(A) 1 (B) 2 (C) 3 (D) 4 [1]

SECTION E

This section comprises 2 long answer questions of 5 marks each.

16. (a) (i) With the help of a circuit diagram (described in words), explain the working of a full-wave rectifier using a centre-tapped transformer. Describe the input and output waveforms. 5
(ii) The secondary of the transformer gives 12 V (rms) between the centre tap and each end. Taking the forward drop of each silicon diode as 0.70 V, find the peak output voltage and the fundamental frequency of the output for a 50 Hz input.

OR

(b) (i) Explain how a p-n junction is formed, and how the depletion layer and the barrier potential change under forward and reverse bias.
(ii) The depletion layer of a silicon junction is 1.0 μm wide and the barrier potential is 0.70 V. Estimate the average electric field in the depletion layer, and the energy an electron from the n-side needs to cross the barrier.

17. (a) (i) How are energy bands formed in a solid? Using the energy band picture, distinguish between conductors, semiconductors and insulators. 5
(ii) At room temperature the intrinsic carrier concentration of silicon is $1.0 \times 10^{16}\ \text{m}^{-3}$. A doped sample has a hole concentration of $4.0 \times 10^{22}\ \text{m}^{-3}$. Find its electron concentration and state the type of semiconductor.

OR

(b) (i) Explain how n-type and p-type semiconductors are obtained, showing the positions of the donor and acceptor energy levels.
(ii) Why does the conductivity of a semiconductor increase with temperature, while that of a metal decreases?

END OF THE QUESTION PAPER

ANSWER KEY — SECTION A

Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
(D)	(A)	(C)	(B)	(A)	(C)	(B)	(D)

MARKING SCHEME AND WORKED SOLUTIONS

Marks for each step are shown in brackets, as in the CBSE marking scheme. Any correct alternative method earns full marks.

Q1. Answer (D). Phosphorus is pentavalent: its fifth electron is donated to the conduction band.

Q2. Answer (A). Each broken bond gives one free electron and one hole: $n_e = n_h = n_i$.

Q3. Answer (C). Silicon: $E_g \approx 1.1$ eV (germanium ≈ 0.7 eV; insulators more than 3 eV).

Q4. Answer (B). Trivalent acceptor atoms create holes, which outnumber the thermally produced electrons.

Q5. Answer (A). The applied voltage opposes the barrier potential, so the barrier falls and the depletion layer narrows.

Q6. Answer (C). Both halves of each cycle give an output pulse: 2 × 50 = 100 Hz.

Q7. Answer (B). A is true (more electron-hole pairs at higher temperature). R is true but is about doping, not temperature. Answer (B).

Q8. Answer (D). The crystal as a whole is neutral (every hole is balanced by a negative acceptor ion), so A is false; holes far outnumber free electrons, so R is false. Answer (D).

Q9. (2 marks) Answer: $n_h \approx 5.0 \times 10^{21}$ m^{-3}; $n_e = 2.0 \times 10^{10}$ m^{-3}; p-type.
$N_A = 5.0 \times 10^{28}/10^7 = 5.0 \times 10^{21}$ m^{-3}, so $n_h \approx 5.0 \times 10^{21}$ m^{-3}. [1]
$n_e = n_i^2/n_h = 10^{32}/5.0 \times 10^{21} = 2.0 \times 10^{10}$ m^{-3}; p-type (boron is trivalent). [1]

Q10. (2 marks) Answer: (a) diffusion leaves ions; field and drift balance; (b) no carriers at 0 K.
(a) Electrons diffuse from the n-side to the p-side and holes from the p-side to the n-side, leaving uncovered positive donor ions on the n-side and negative acceptor ions on the p-side near the junction: this region with no free carriers is the depletion region. [1]
These ions set up an electric field from n to p, which drives a drift current opposite to the diffusion current; in equilibrium the two balance, and the potential difference across the region is the barrier potential (about 0.7 V for Si). [1]
OR (b) At 0 K all electrons are in the valence band and the conduction band is empty, so there are no free charge carriers: it is an insulator. [1] At room temperature some electrons gain enough thermal energy to cross the small band gap, creating free electrons and holes, so it conducts a little. [1]

Q11. (2 marks) Answer: 21.5 mA; practically zero.
I = (5.0 − 0.70)/200 = 4.3/200 = 21.5 mA. [1]
Reversed, the diode is reverse biased: only a tiny reverse current (of the order of μA or less) flows — practically zero. [1]

Q12. (3 marks) Answer: (a) conducts in one half cycle only; (b) $r_d = 5.0\ \Omega$.

(a) The AC is applied (usually through a transformer) to a diode in series with a load resistor R_L; the output is taken across R_L. [1]

During the half cycle that makes the diode's p-side positive it is forward biased and conducts, so the voltage appears across R_L; during the other half it is reverse biased, no current flows and the output is zero. [1]

Input: a sine wave. Output: only the positive half cycles, with gaps between them — a pulsating DC of the same frequency as the input. [1]

OR (b) (i) Forward bias: hardly any current until the threshold (knee) voltage (about 0.7 V for Si), then the current rises steeply. Reverse bias: a very small current, almost constant, until breakdown. [2]

(ii) $r_d = \Delta V/\Delta I = (0.75 - 0.70)/(20 - 10) \times 10^{-3} = 5.0\ \Omega$. [1]

Q13. (3 marks) Answer: (i) 0.10 A, 0; (ii) 0.10 A; (iii) 0, 0.10 A; 0.10 A.

(i) D_1 (ideal, forward) acts as a closed switch: $I_1 = 10/100 = 0.10$ A. D_2 (reverse) acts as an open switch: $I_2 = 0$. [1]

(ii) $I = I_1 + I_2 = 0.10$ A. [1]

(iii) Now D_2 conducts and D_1 does not: $I_2 = 0.10$ A, $I_1 = 0$, battery current still 0.10 A. [1]

Q14. (3 marks) Answer: (i) widens, barrier rises; (ii) minority carriers only; (iii) breakdown.

(i) The applied voltage adds to the barrier potential, so the barrier rises and the depletion layer widens. [1]

(ii) The reverse current is carried only by minority carriers drifting across the junction; their number depends on temperature, not on the voltage, so the current soon saturates at a small value. [1]

(iii) At the breakdown voltage the reverse current rises suddenly and sharply; unless it is limited, the diode may be damaged. [1]

Q15. (4 marks) Answer: (I) C; (II) A; (III) D; (IV) B.

(I) (C) Both half cycles reach the load in the same direction: full-wave rectification. [1]

(II) (A) Two pulses per input cycle: 100 Hz. [1]

(III) (D) It charges near the peaks and discharges slowly through the load between them, filling in the gaps. [1]

(IV) (B) In each half cycle two diodes, in opposite arms, are forward biased. [1]

Q16. (5 marks) Answer: (a) ≈ 16.3 V; 100 Hz; (b) ≈ 7.0×10^5 V m^{-1}; 0.70 eV.

(a) (i) The two ends of the secondary go to the p-sides of diodes D_1 and D_2, whose n-sides are joined; the load is connected between this junction and the centre tap. [1] In one half cycle end A is positive: D_1 conducts and D_2 is reverse biased; in the next half cycle B is positive and D_2 conducts. In both, the current flows through the load in the same direction. [1] Output: every half cycle appears as a positive pulse — a pulsating DC of twice the input frequency. [1]

(ii) Peak across each half: $12\sqrt{2} \approx 17.0$ V; output peak ≈ 17.0 − 0.70 ≈ 16.3 V. [1] Output frequency = $2 \times 50 = 100$ Hz. [1]

OR (b) (i) Diffusion of majority carriers across the junction leaves a layer of immobile ions, positive on the n-side and negative on the p-side (the depletion layer), with an electric field from n to p that opposes further diffusion: the barrier potential. [1] Forward bias lowers the barrier and narrows the layer, so a large diffusion current flows. [1] Reverse bias raises the barrier and widens the layer; only the small drift current of minority carriers flows. [1]

(ii) $E \approx V/d = 0.70/1.0 \times 10^{-6} = 7.0 \times 10^5$ V m^{-1}. [1] An electron needs 0.70 eV (≈ 1.1×10^{-19} J) to cross the barrier from the n-side. [1]

Q17. (5 marks) Answer: (a) $n_e = 2.5 \times 10^9\ m^{-3}$; p-type; (b) donor and acceptor levels.

(a) (i) When atoms are brought close together, each energy level of an isolated atom splits into a very large number of closely spaced levels — a band; the highest filled band is the valence band and the next one the conduction band. [1] Conductors: the bands overlap (or the conduction band is partly filled), so free electrons are always present. Semiconductors: a small gap (E_g < 3 eV, e.g. Si 1.1 eV) which some electrons cross at room temperature. Insulators: a large gap (E_g > 3 eV) that electrons cannot cross. [2]

(ii) $n_e = n_i^2/n_h = 10^{32}/(4.0 \times 10^{22}) = 2.5 \times 10^9\ m^{-3}$. [1] Holes are the majority carriers: p-type. [1]

OR (b) (i) n-type: a pentavalent atom (P, As) uses four electrons in bonds; the fifth is so loosely bound that its level (the donor level) lies just below the conduction band (about 0.01 to 0.05 eV), and it easily becomes free. [1½] p-type: a trivalent atom (B, Al, In) leaves one bond incomplete — a hole; the acceptor level lies just above the valence band, and electrons from the valence band easily fill it, leaving holes there. [1½]

(ii) In a semiconductor a rise in temperature frees many more electron-hole pairs, and this increase in carrier numbers outweighs the extra collisions, so the conductivity rises. In a metal the number of free electrons is fixed; more vibration of the ions only means more collisions (smaller relaxation time), so the conductivity falls. [2]

All questions are original and © Master Testing Agency. Free to download and use for personal practice; not for resale. Every answer in this paper was checked independently by computer: carrier concentrations from $n_e n_h = n_i^2$, diode circuits with a diode model, rectifier outputs by sampling the waveform and counting its peaks.